FIG. 1

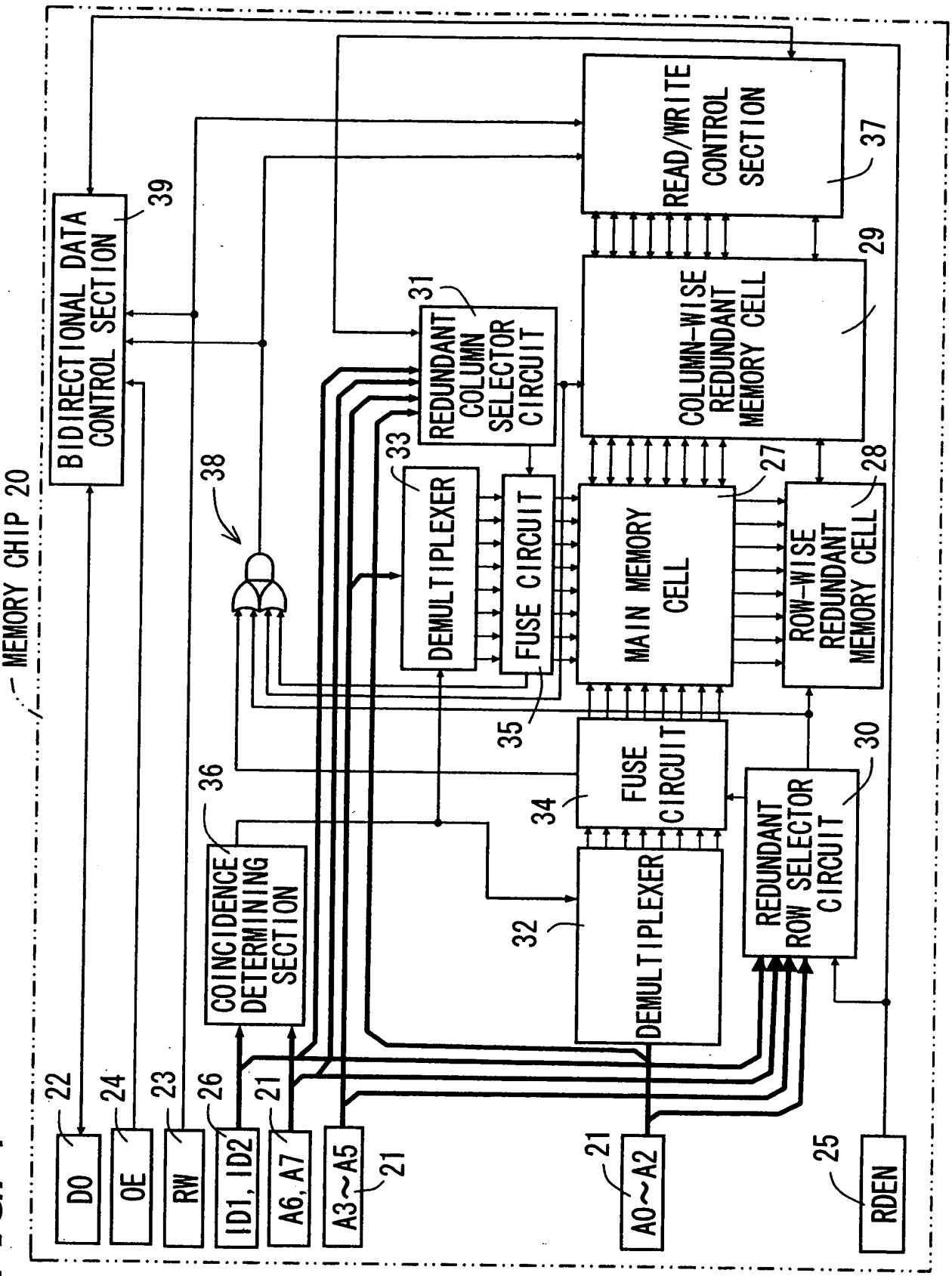

MEMORY CHIP 20
BIDIRECTIONAL DATA CONTROL SECTION
39
READ/WRITE CONTROL SECTION
37
COLUMN-WISE REDUNDANT MEMORY CELL
29
REDUNDANT COLUMN SELECTOR CIRCUIT
31
DEMULTIPLEXER
33
FUSE CIRCUIT
35
MAIN MEMORY CELL
27
ROW-WISE REDUNDANT MEMORY CELL
28
38
FUSE CIRCUIT
34
REDUNDANT ROW SELECTOR CIRCUIT
30
DEMULTIPLEXER
32
COINCIDENCE DETERMINING SECTION
36
D0
22
OE
24
RW
23
ID1, ID2
26
A6, A7
21
A3~A5
21
A0~A2
21
RDEN
25

FIG. 2

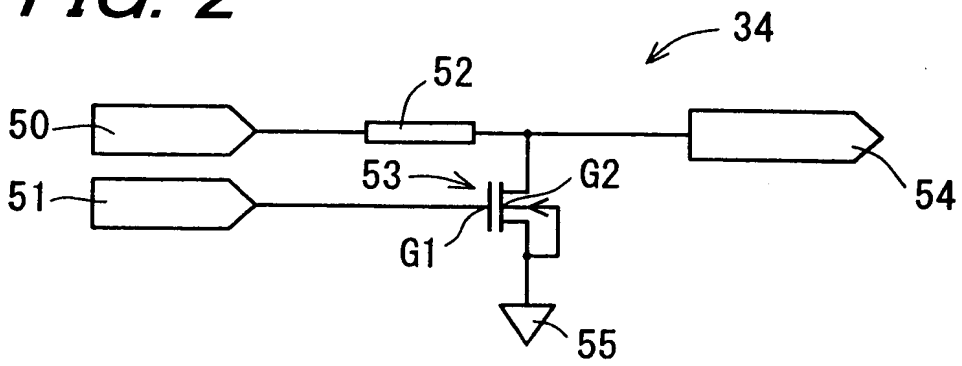


FIG. 3

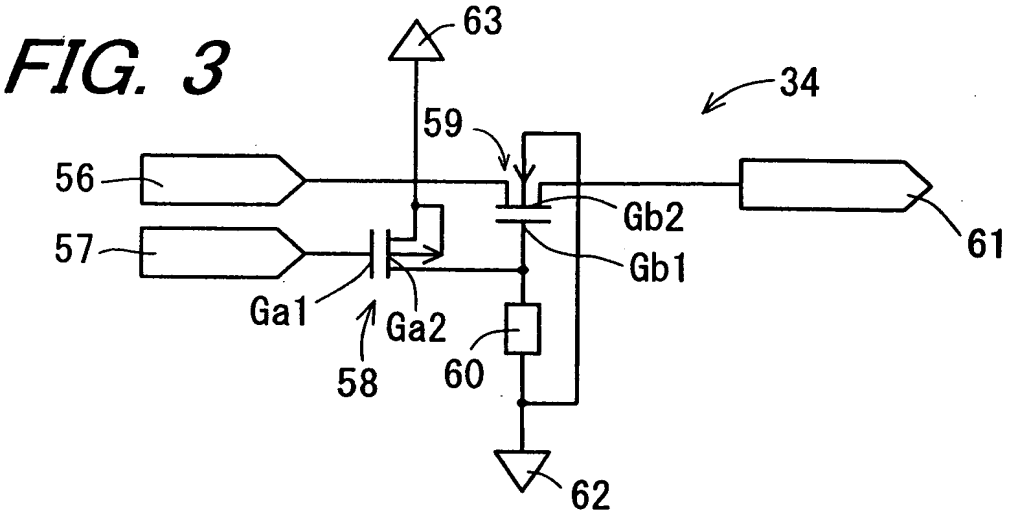


FIG. 4

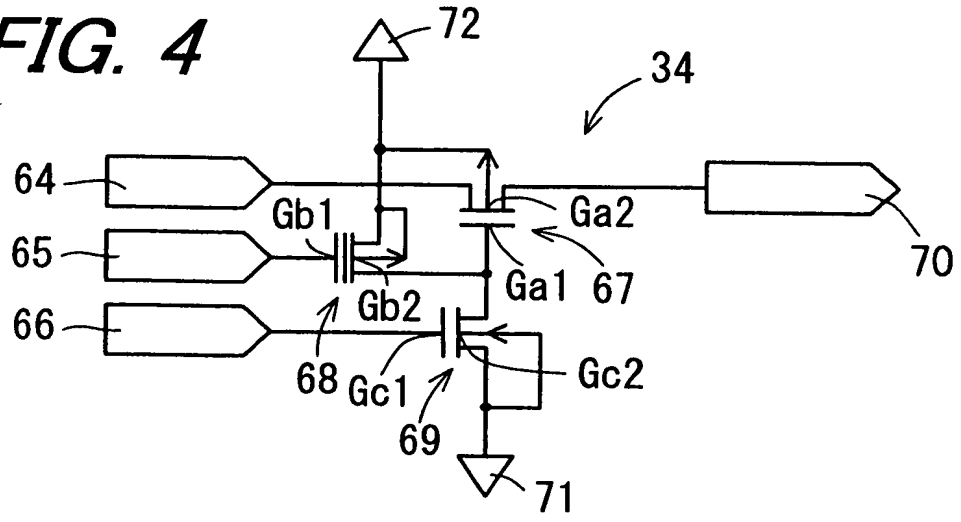


FIG. 5A

RDEN	A0～A2	A3	A4, A5	A6, A7
H	ROW (COLUMN)-WISE REDUNDANT RESISTOR VALUE	ROW OR COLUMN	COMMAND NUMBER	ID NUMBER

A3=0 : REDUNDANT ROW-BASED RELIEF
A3=1 : REDUNDANT COLUMN-BASED RELIEF

A4=1, A5=0 : REDUNDANCY COMMAND 1
A4=0, A5=1 : REDUNDANCY COMMAND 2

FIG. 5B

RDEN	A0～A5	A6, A7
L	ADDRESS	ID NUMBER

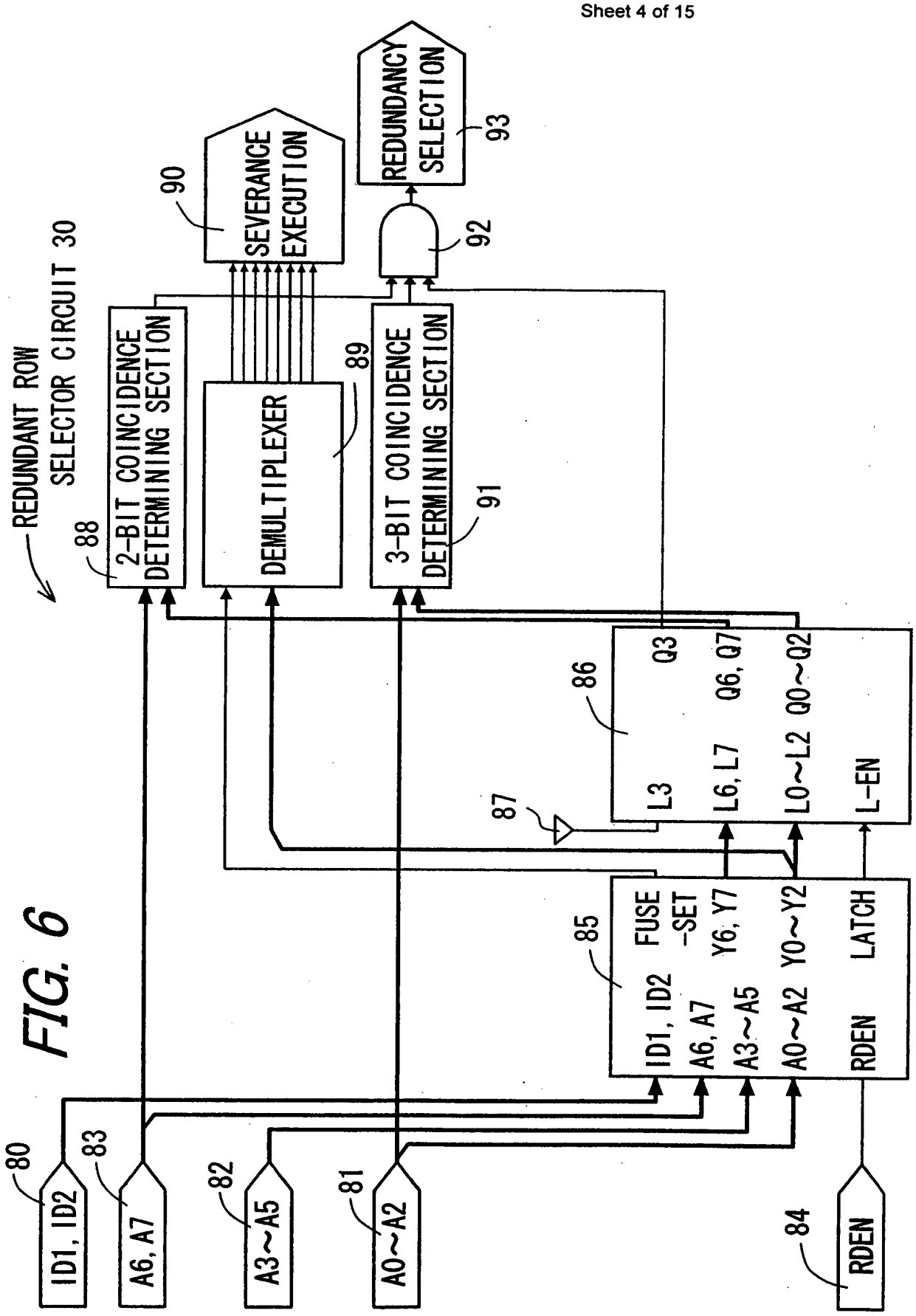

REDUNDANT ROW SELECTOR CIRCUIT 30
2-BIT COINCIDENCE DETERMINING SECTION
88
DEMULTIPLEXER
89
3-BIT COINCIDENCE DETERMINING SECTION
91
SEVERANCE EXECUTION
90
REDUNDANCY SELECTION
93
92
86
Q3
Q6, Q7
Q0~Q2
L3
L6, L7
L0~L2
L-EN
87
85
ID1, ID2
FUSE -SET
A6, A7
Y6, Y7
A3~A5
Y0~Y2
A0~A2
LATCH
RDEN
80
ID1, ID2
83
A6, A7
82
A3~A5
81
A0~A2
84
RDEN

FIG. 6

FIG. 7

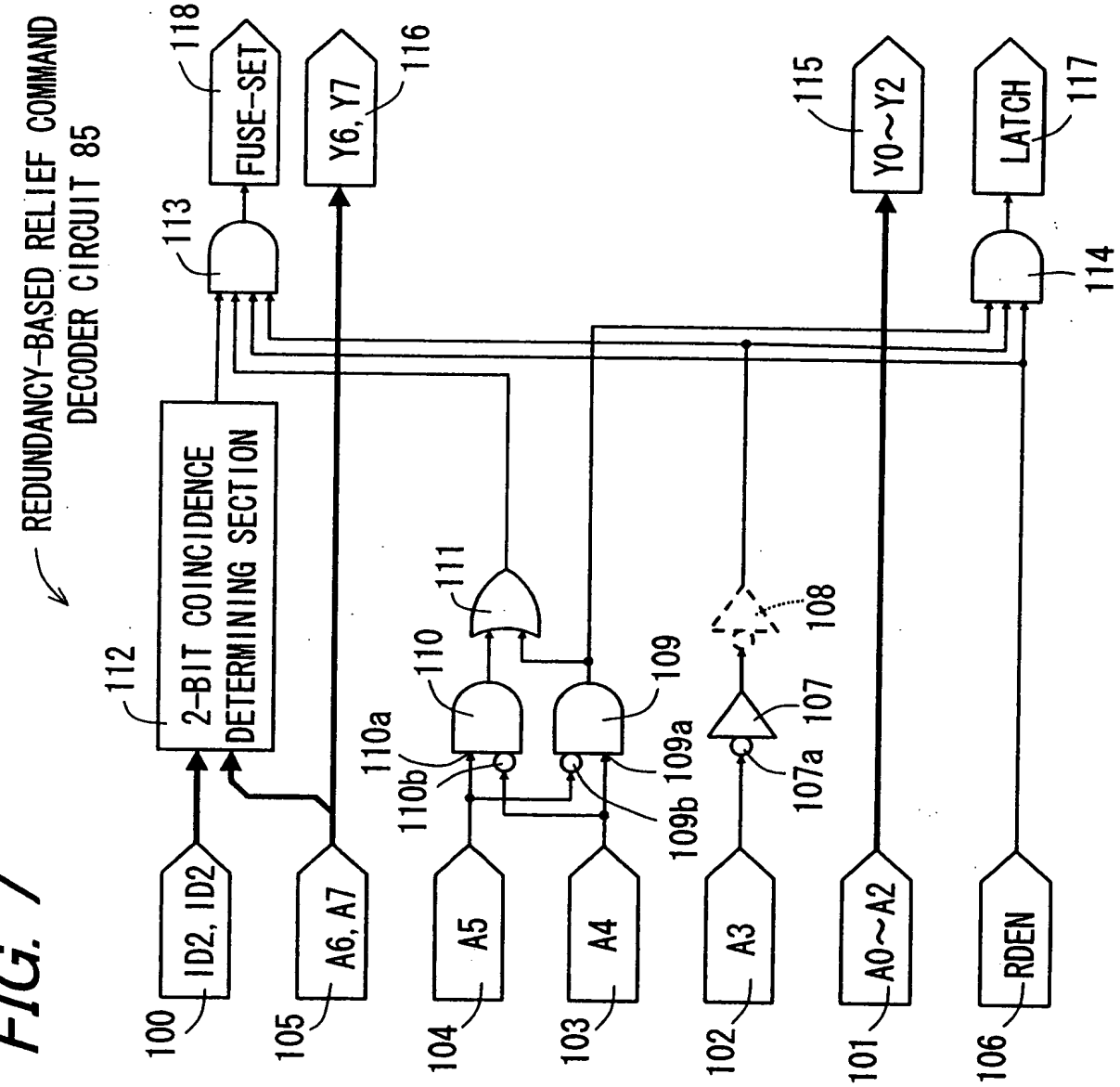

REDUNDANCY-BASED RELIEF COMMAND DECODER CIRCUIT 85
2-BIT COINCIDENCE DETERMINING SECTION
112
FUSE-SET
118
Y6, Y7
116
113
Y0~Y2
115
LATCH
117
114
111
110
110a
110b
109
109a
108
107
107a
ID2, ID2
100
A6, A7
105
A5
104
A4
103
A3
102
A0~A2
101
RDEN
106

FIG. 8

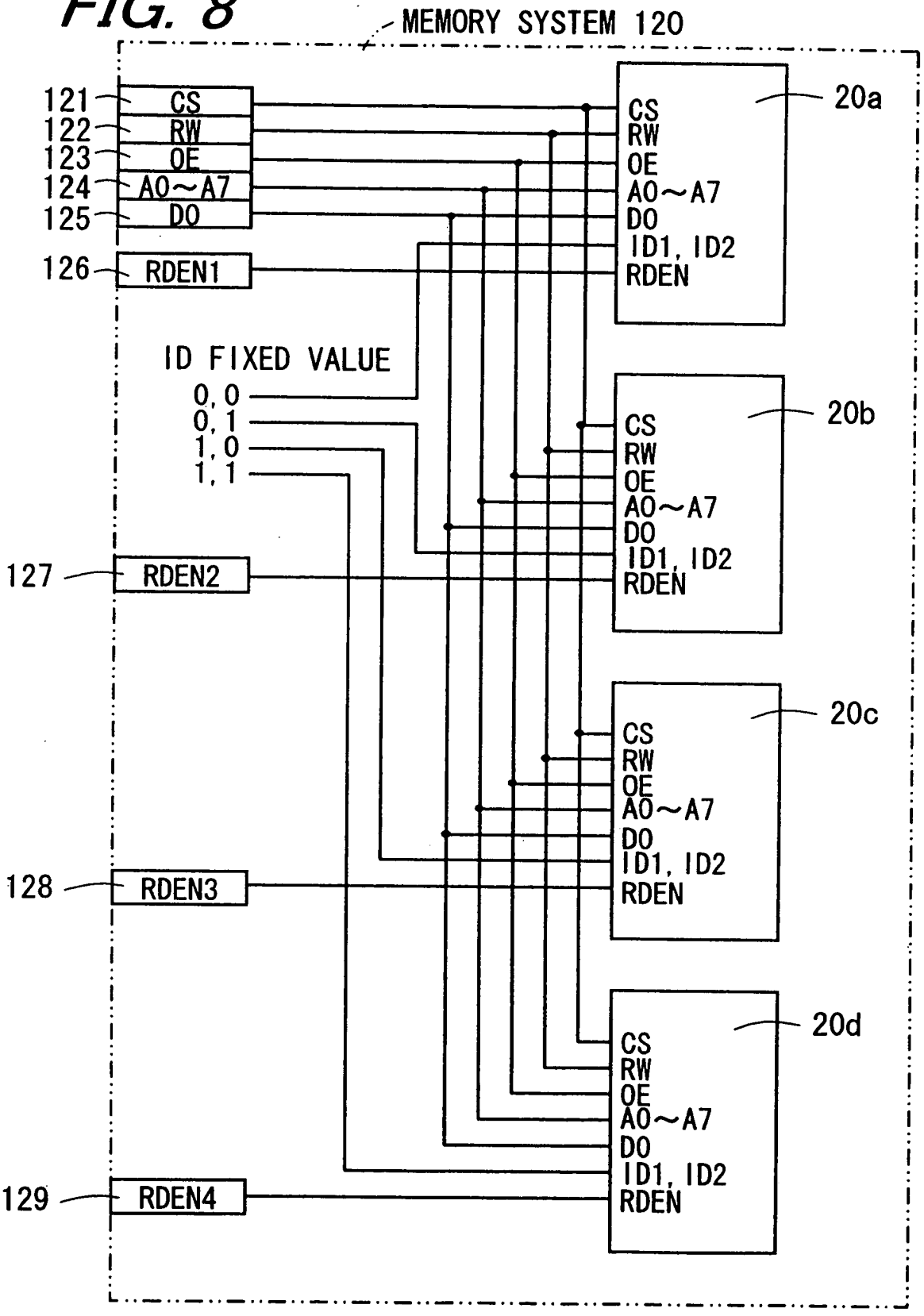

MEMORY SYSTEM 120
121
CS
122
RW
123
OE
124
A0~A7
125
DO
126
RDEN1
ID FIXED VALUE
0, 0
0, 1
1, 0
1, 1
127
RDEN2
128
RDEN3
129
RDEN4
20a
20b
20c
20d
CS
RW
OE
A0~A7
DO
ID1, ID2
RDEN

FIG. 9

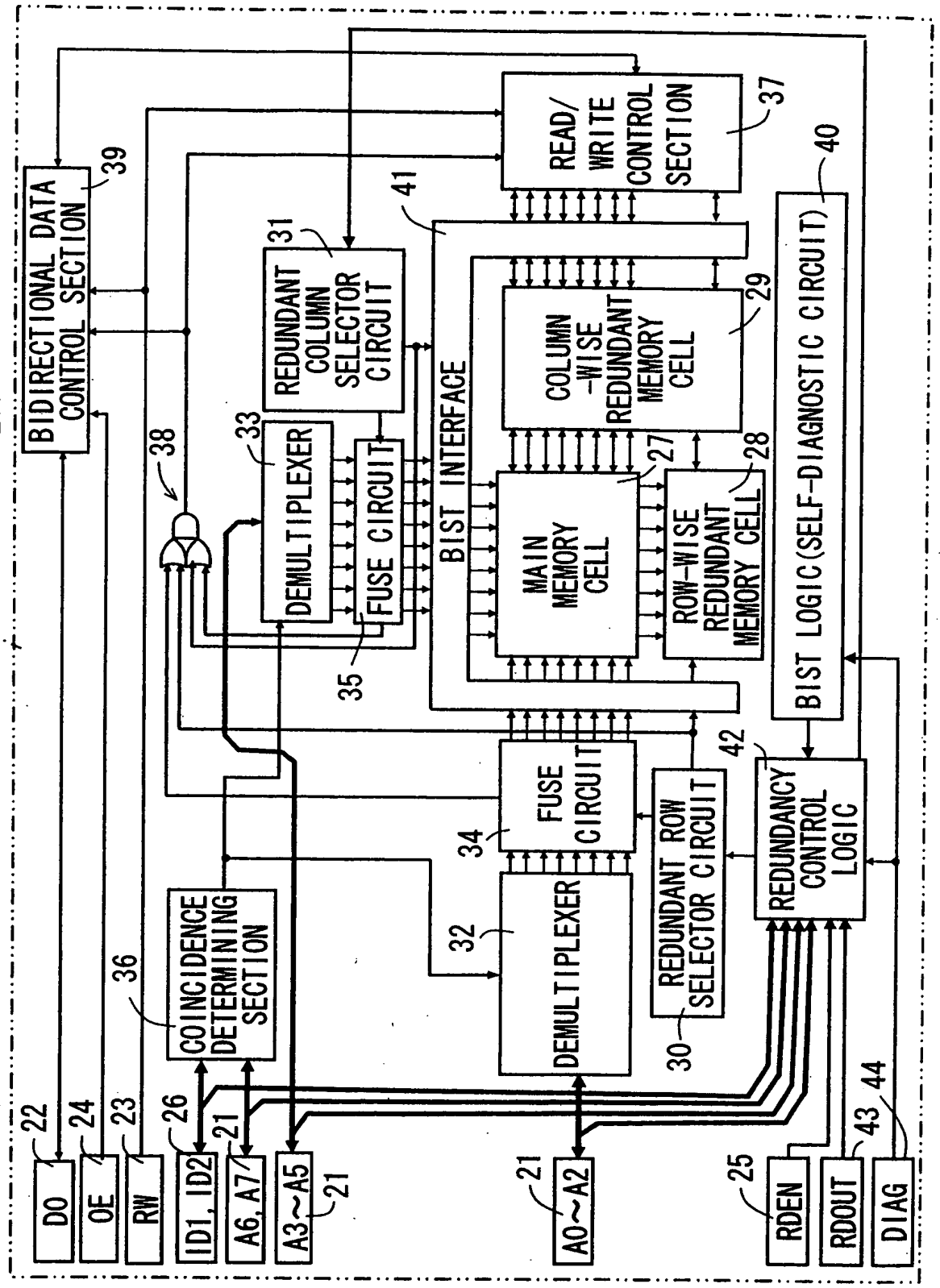

MEMORY CHIP 200
BIDIRECTIONAL DATA CONTROL SECTION
39
READ/ WRITE CONTROL SECTION
37
40
41
REDUNDANT COLUMN SELECTOR CIRCUIT
31
COLUMN -WISE REDUNDANT MEMORY CELL
29
BIST INTERFACE
38
33
DEMULTIPLEXER
FUSE CIRCUIT
35
MAIN MEMORY CELL
27
ROW-WISE REDUNDANT MEMORY CELL
28
BIST LOGIC(SELF-DIAGNOSTIC CIRCUIT)
42
FUSE CIRCUIT
34
REDUNDANCY CONTROL LOGIC
REDUNDANT ROW SELECTOR CIRCUIT
30
32
DEMULTIPLEXER
36
COINCIDENCE DETERMINING SECTION
22
24
23
26
21
21
21
25
43
44
DO
OE
RW
ID1, ID2
A6, A7
A3~A5
A0~A2
RDEN
RDOUT
DIAG

FIG. 10A

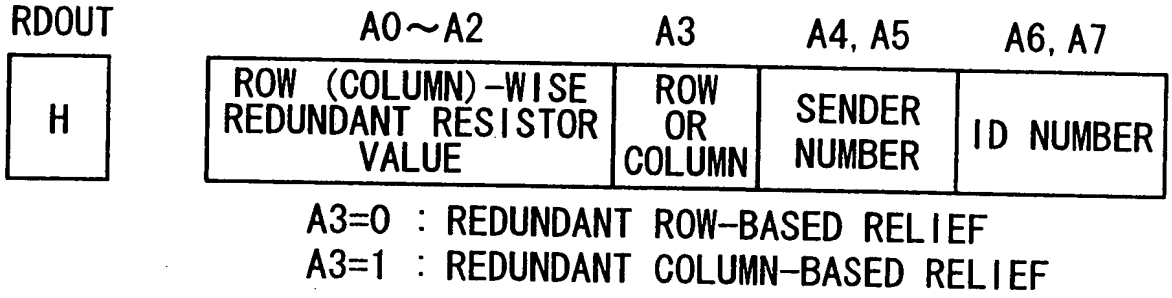


FIG. 10B

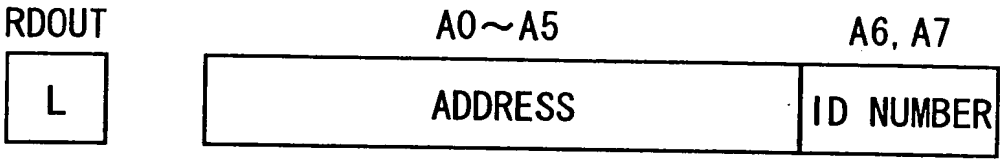


FIG. 11

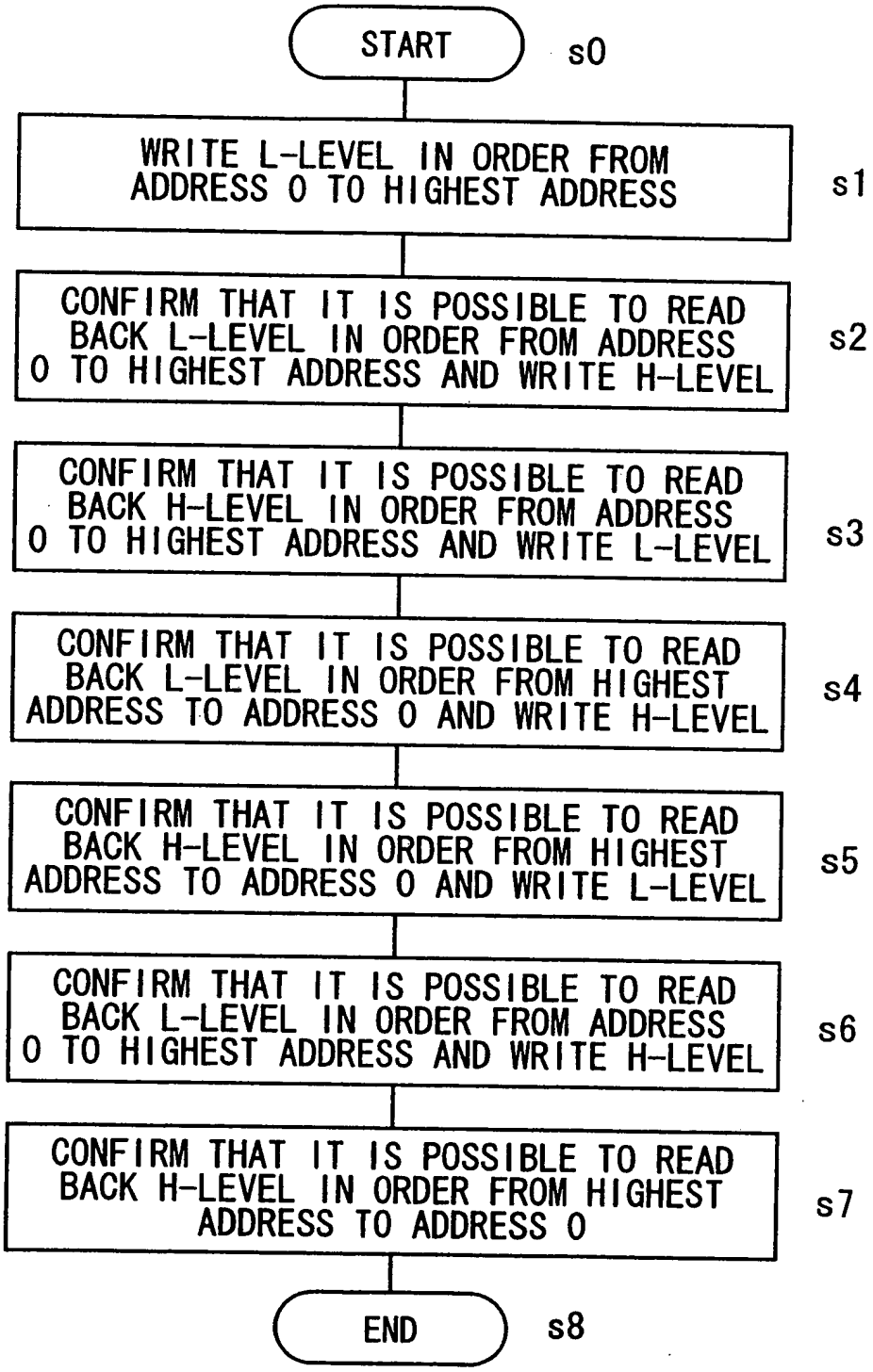

START
s0
WRITE L-LEVEL IN ORDER FROM ADDRESS 0 TO HIGHEST ADDRESS
s1
CONFIRM THAT IT IS POSSIBLE TO READ BACK L-LEVEL IN ORDER FROM ADDRESS 0 TO HIGHEST ADDRESS AND WRITE H-LEVEL
s2
CONFIRM THAT IT IS POSSIBLE TO READ BACK H-LEVEL IN ORDER FROM ADDRESS 0 TO HIGHEST ADDRESS AND WRITE L-LEVEL
s3
CONFIRM THAT IT IS POSSIBLE TO READ BACK L-LEVEL IN ORDER FROM HIGHEST ADDRESS TO ADDRESS 0 AND WRITE H-LEVEL
s4
CONFIRM THAT IT IS POSSIBLE TO READ BACK H-LEVEL IN ORDER FROM HIGHEST ADDRESS TO ADDRESS 0 AND WRITE L-LEVEL
s5
CONFIRM THAT IT IS POSSIBLE TO READ BACK L-LEVEL IN ORDER FROM ADDRESS 0 TO HIGHEST ADDRESS AND WRITE H-LEVEL
s6
CONFIRM THAT IT IS POSSIBLE TO READ BACK H-LEVEL IN ORDER FROM HIGHEST ADDRESS TO ADDRESS 0
s7
END
s8

FIG. 12

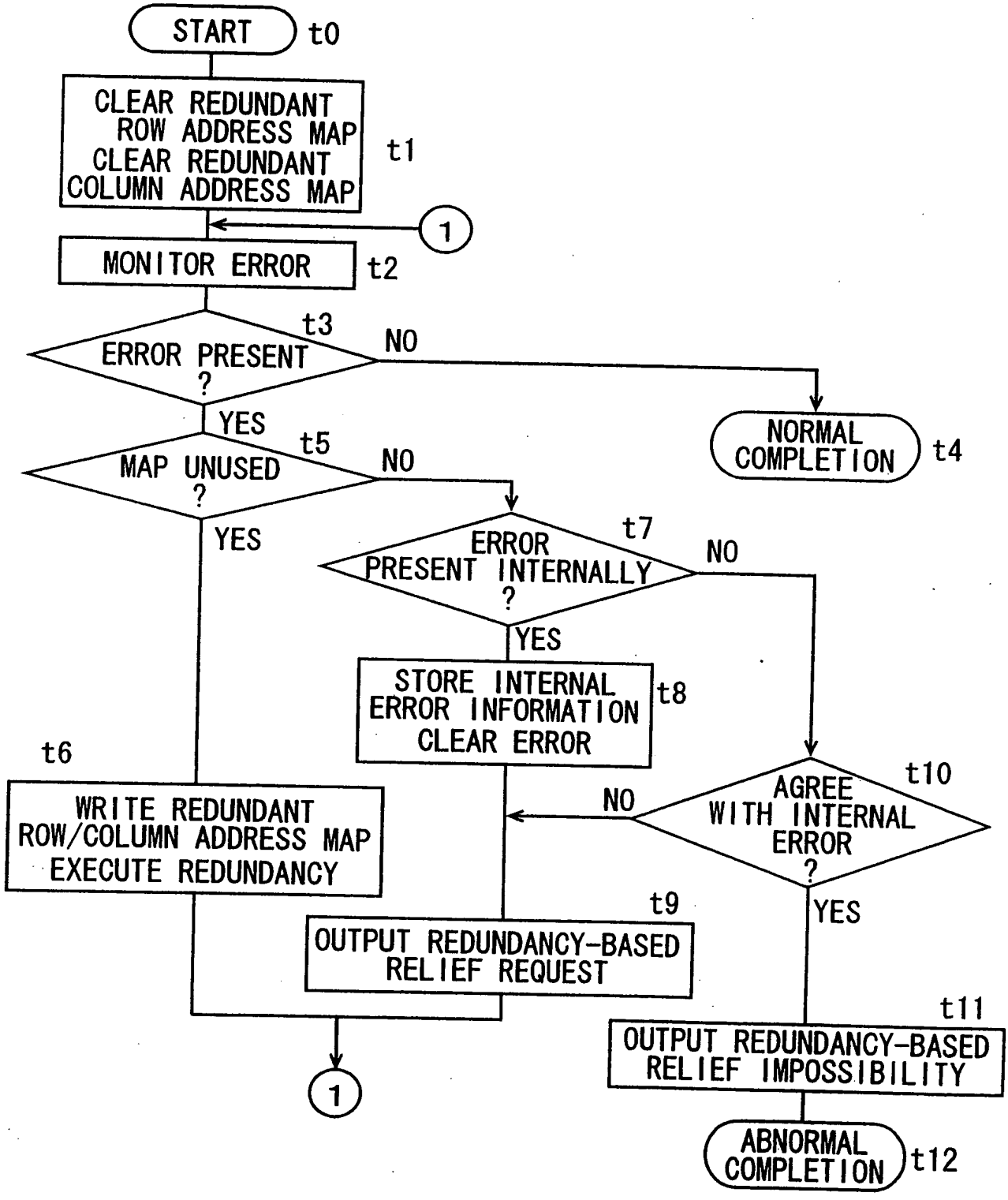

START
t0
CLEAR REDUNDANT ROW ADDRESS MAP
CLEAR REDUNDANT COLUMN ADDRESS MAP
t1
1
MONITOR ERROR
t2
t3
ERROR PRESENT ?
NO
NORMAL COMPLETION
t4
YES
t5
MAP UNUSED ?
NO
YES
t7
ERROR PRESENT INTERNALLY ?
NO
YES
STORE INTERNAL ERROR INFORMATION
CLEAR ERROR
t8
t6
WRITE REDUNDANT ROW/COLUMN ADDRESS MAP
EXECUTE REDUNDANCY
t10
AGREE WITH INTERNAL ERROR ?
NO
YES
t9
OUTPUT REDUNDANCY-BASED RELIEF REQUEST
t11
OUTPUT REDUNDANCY-BASED RELIEF IMPOSSIBILITY
1
ABNORMAL COMPLETION
t12

FIG. 13

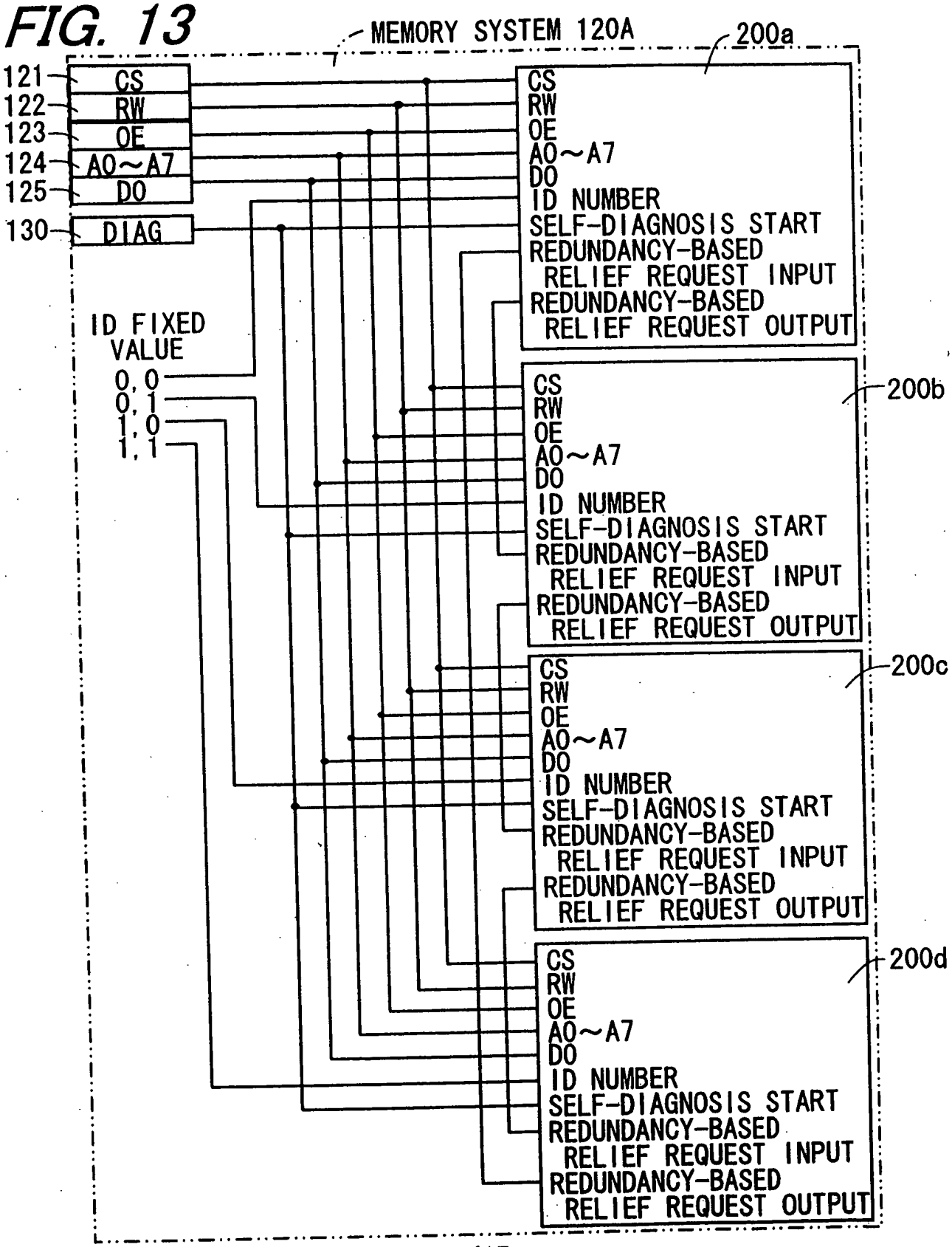

MEMORY SYSTEM 120A
200a
121
122
123
124
125
130
CS
RW
OE
A0~A7
DO
DIAG
ID FIXED VALUE
0,0
0,1
1,0
1,1
ID NUMBER
SELF-DIAGNOSIS START
REDUNDANCY-BASED RELIEF REQUEST INPUT
REDUNDANCY-BASED RELIEF REQUEST OUTPUT
200b
200c
200d

FIG. 14

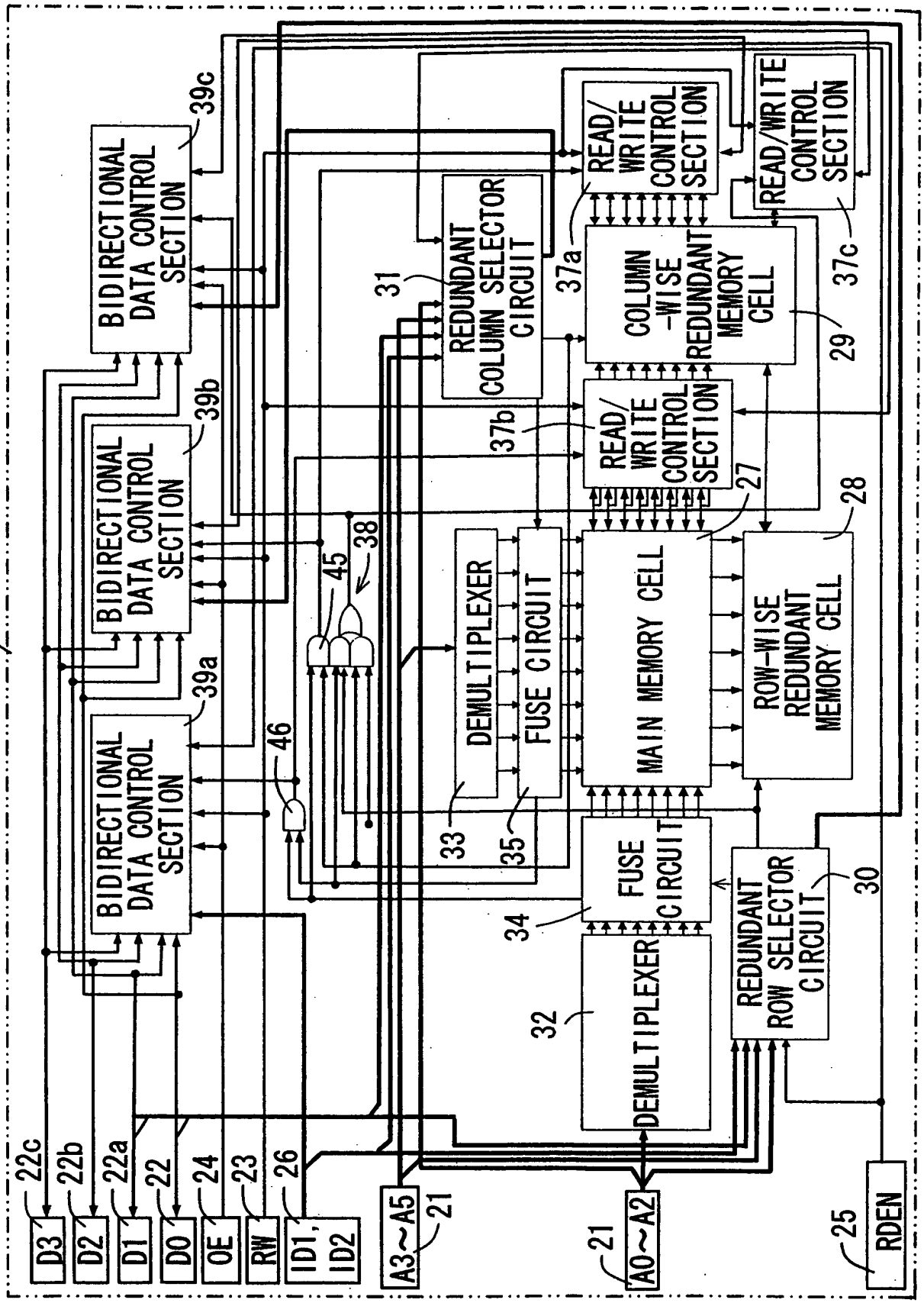

MEMORY CHIP 200A
BIDIRECTIONAL DATA CONTROL SECTION
39c
39b
39a
REDUNDANT COLUMN SELECTOR CIRCUIT
31
READ/WRITE CONTROL SECTION
37a
37b
37c
READ/WRITE CONTROL SECTION
COLUMN-WISE REDUNDANT MEMORY CELL
29
27
28
DEMULTIPLEXER
33
FUSE CIRCUIT
35
MAIN MEMORY CELL
ROW-WISE REDUNDANT MEMORY CELL
45
38
46
FUSE CIRCUIT
34
DEMULTIPLEXER
32
REDUNDANT ROW SELECTOR CIRCUIT
30
D3
D2
D1
D0
OE
RW
ID1, ID2
A3~A5
21
A0~A2
21
RDEN
25
22c
22b
22a
22
24
23
26

FIG. 15

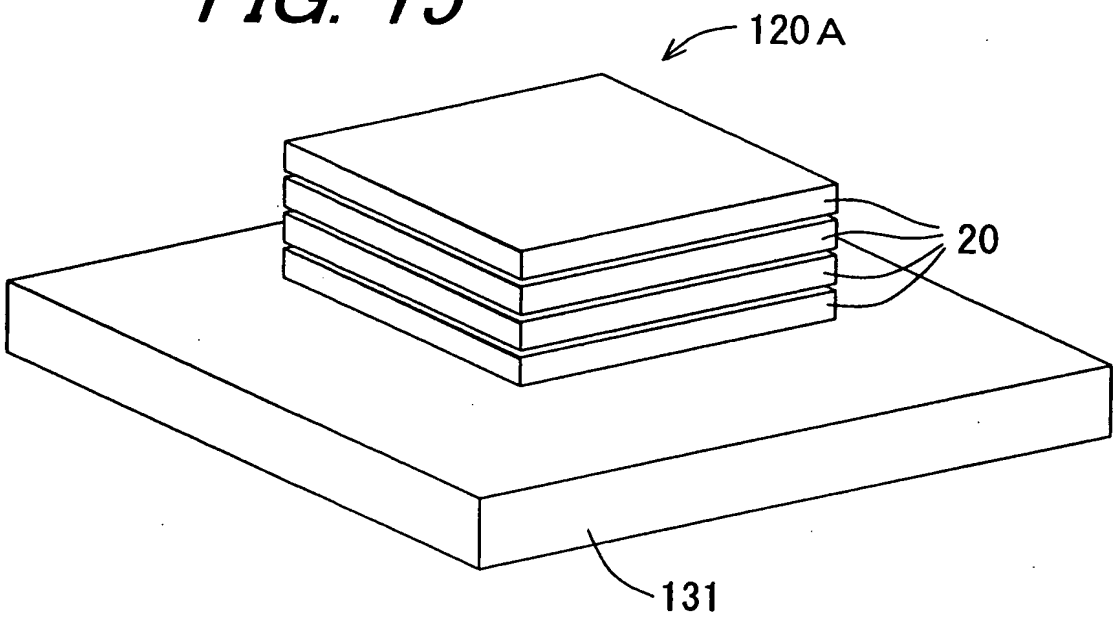


FIG. 16A

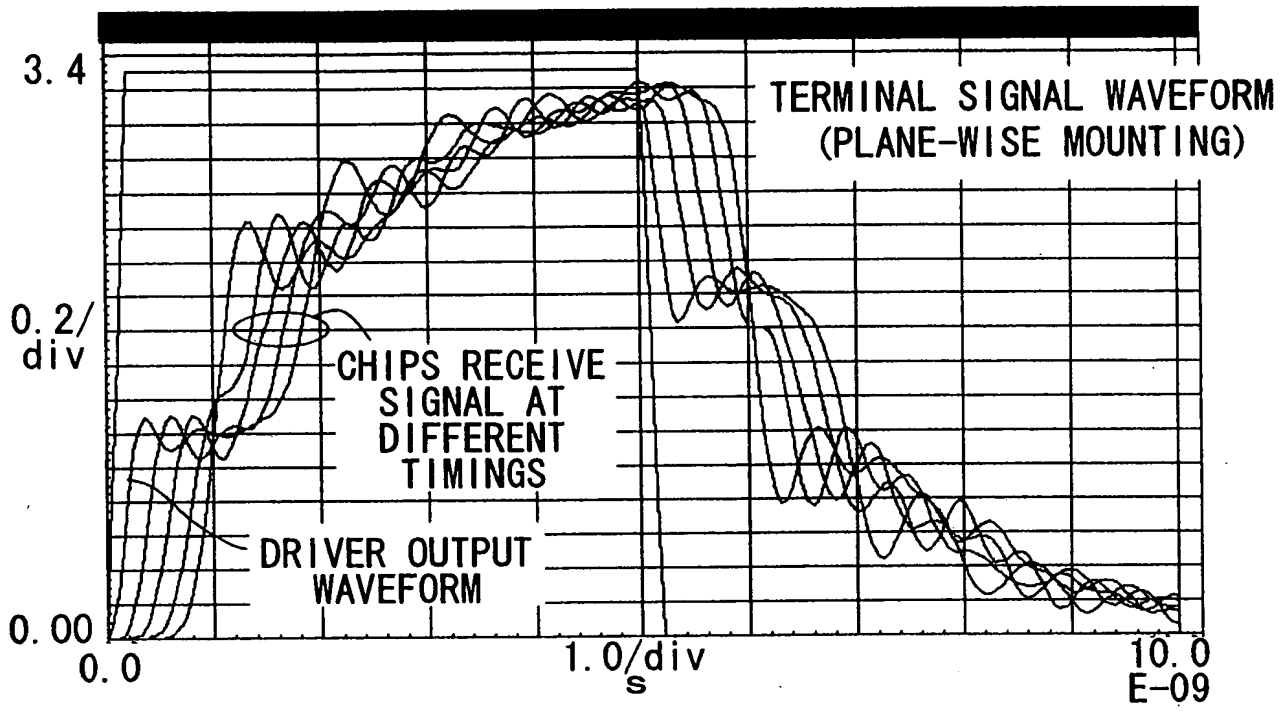


FIG. 16B

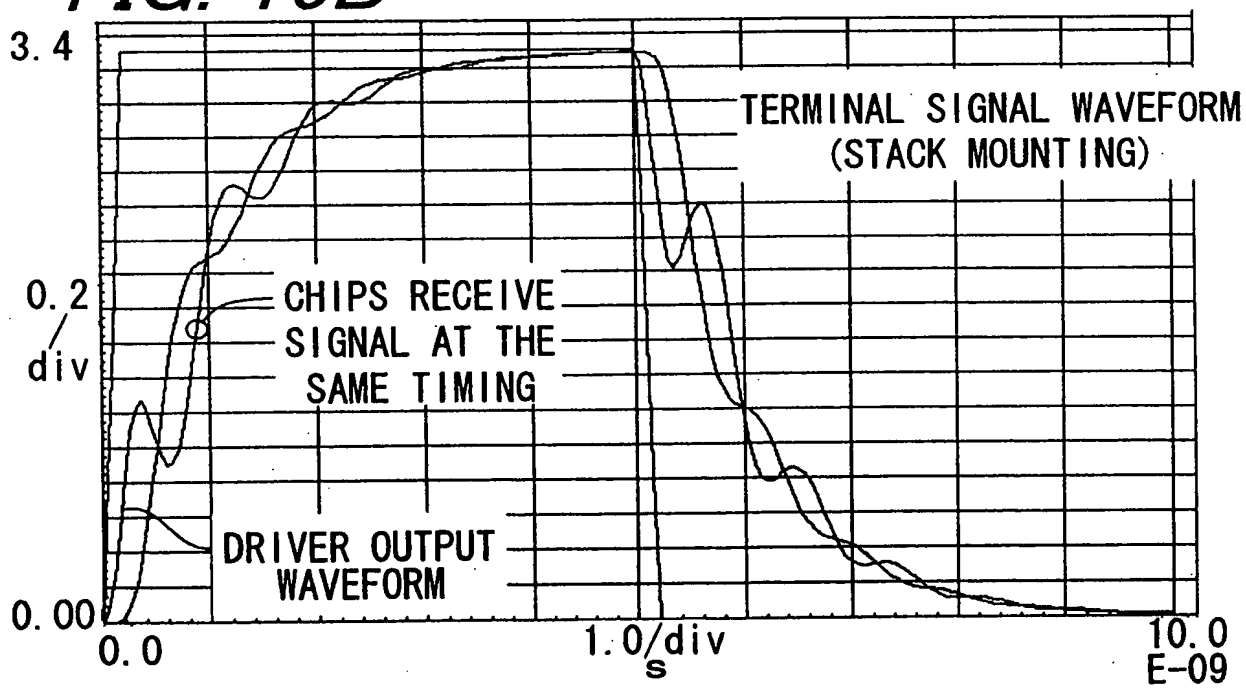
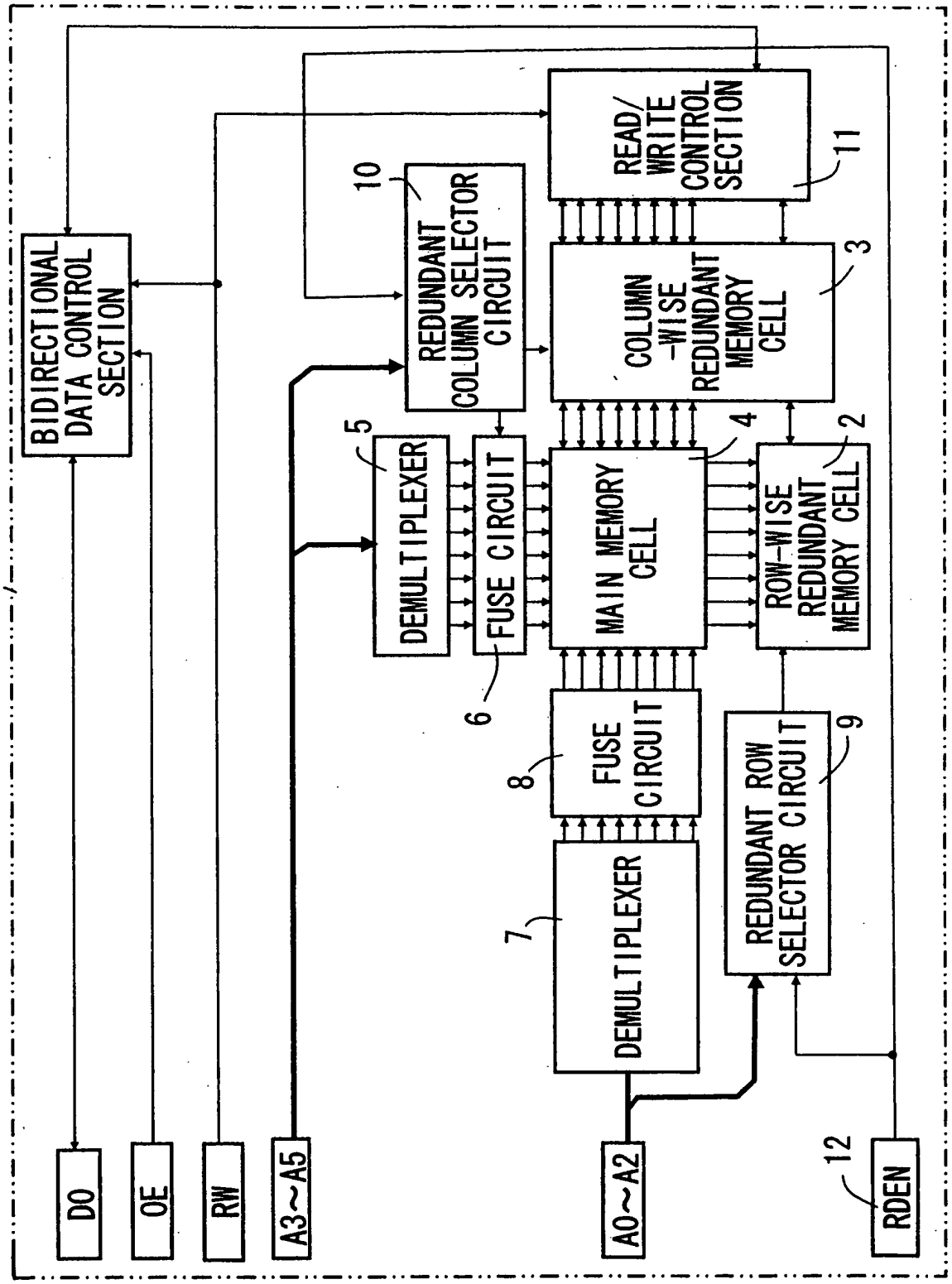


FIG. 17


1
BIDIRECTIONAL DATA CONTROL SECTION
READ/ WRITE CONTROL SECTION
11
10
REDUNDANT COLUMN SELECTOR CIRCUIT
COLUMN -WISE REDUNDANT MEMORY CELL
3
5
DEMULTIPLEXER
FUSE CIRCUIT
6
MAIN MEMORY CELL
4
ROW-WISE REDUNDANT MEMORY CELL
2
8
FUSE CIRCUIT
REDUNDANT ROW SELECTOR CIRCUIT
9
7
DEMULTIPLEXER
12
RDEN
DO
OE
RW
A3~A5
A0~A2